PATTERN GENERATOR FOR SEMICONDUCTOR TEST SYSTEM

ABSTRACT OF THE DISCLOSURE

A pattern generator for semiconductor test system for testing a semiconductor memory device by generating and applying test patterns. The pattern generator is capable of freely generating inversion request signals for inverting the read/write data for specified memory cells for a memory device under test having different numbers of memory cells between X (row) and Y (column) directions. The locations of specified memory cells are on a diagonal line on an array of memory cells in the memory device under test or on a reverse diagonal line which is perpendicular to the diagonal line.